A Novel Design of Compact Out-of-Phase Power Divider With Arbitrary Ratio

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***Abstract*— In a conventional power divider, power dividing network and isolation network are usually independent of each other. To reduce the size of out-of-phase power divider with arbitrary power ratio, coupled microstrip lines are proposed to facilitate power dividing and isolation of a power divider simultaneously in this article. Formulations have been derived for the proposed out-of-phase power divider with arbitrary ratio. Two compact power dividers are implemented on the printed circuit board (PCB) with power ratio $k^2 = 9$ and $k^2 = 1000$. It can be observed that there is a satisfactory agreement between the simulated and measured results.**

***Index Terms*— Arbitrary power ratio, coupled microstrip lines, image impedance, out-of-phase, power divider.**

I. Introduction

As 5G technology develops, miniaturization becomes an important task in designing RF front-end [1], [2]. Power divider [3] is an important passive component to compose a complex RF front-end. Conventional two-way Gysel [4] power divider is usually applied to implement multifunction, such as arbitrary power ratio, arbitrary terminal real impedance [5], and in-/out-of-phase output [6]. This is because both power dividing and isolation networks are related to half wavelength electrical length at the central frequency. However, the relationship between power dividing and isolation networks has not been discussed explicitly.

In our previous work [7], we have discussed the relationship between power dividing and isolation networks of a balanced-to-balanced power divider with arbitrary ratio in Y matrix. In this article, we will analyze the relationship between power dividing and isolation networks of a single-ended power divider with arbitrary ratio. The leading objective is to provide the demanding compact feature when designing an out-of-phase power divider.

Balanced or differential circuits have attracted many attention in recent years for better noise performance, linearity, and stability [8]. Before all-balanced RF-ends are widely used in transceivers, Balun and out-of-phase power divider are considered as important tools to connect single-ended components with balanced components. Balun usually has poor isolation performance for being devoid of isolated resistors. Instead, out-of-phase power divider with a resistor can provide feasible isolation performance.

Out-of-phase power divider has been discussed in many works previously. Slot, double-sided parallel-strip lines (DSPSLs), substrate integrated waveguide (SIW), coupled microstrip lines, and hybrid ring with coupled microstrip lines [9]–[13] have been adopted to compose an out-of-phase power divider. A T-junction formed by a slotline and a microstrip line enabling wideband microstrip to slotline transitions [9] is employed to achieve an out-of-phase signal division over a wide frequency range. However, its isolation is unsatisfactory without any isolated resistors. To preserve the out-of-phase feature between the two output ports, DSPSLs are employed in [10]. Nevertheless, when a DSPSL circuit with antiphase ports connects to a microstrip circuit, the ground plane is difficult to be determined. In [11], resistive coupling slots are realized on the lateral half mode SIW (HMSIW) Y-junctions and the vertical HMSIW Y-junctions using isolation resistors to obtain good isolation among four output ports and impedance matching therein. However, SIW is not a compact structure for planar power dividers, even for HMSIW. Two pairs of parallel-coupled lines in addition to the conventional Wilkinson structure have been utilized to obtain out-of-phase response by controlling the status of the two terminals in one of the coupled line pair (either open-ended or short-ended) in [12]. However, its size is not compact. A small-sized ring hybrid [13] with arbitrary power dividing, arbitrary terminal real impedance was proposed to realize the out-of-phase output. To achieve a more compact structure, we introduce a novel methodology on a new structure. Coupled microstrip lines have been used to provide the $\pm 90^\circ$ impedance transformer [12], [13] in power dividing networks or isolation networks to design power dividers. However, to our best knowledge, coupled microstrip lines are seldom used in power dividing networks and isolation networks simultaneously. In our design, we will use coupled microstrip lines in power dividing networks and isolation networks to attain a more compact power divider using one resistor with arbitrary ratio.

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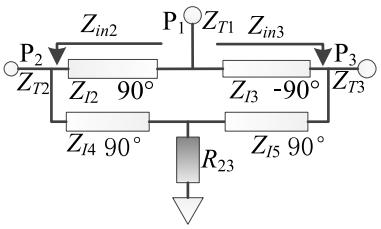


Fig. 1. Generalized two-way Gysel out-of-phase power divider model with one isolation resistor.

In [14]–[17], research on filtering power dividers attempt to reduce the size of complex RF front-end by multifunction components. The proposed out-of-phase power divider can provide multiple functions, especially arbitrary terminal real impedance and arbitrary power ratio.

This article is organized as follows. Section II presents a method to analyze the out-of-phase power divider. Section III gives a distinct process to determine values of the resistor and image impedance of coupled microstrip lines together with other main parameters for two kinds of power dividers. The implementation and performance of a power divider will be demonstrated in Section IV.

II. Methodology of Proposed Power Divider

A. New Method for Power Divider Analysis

As we know, S-parameters of an out-of-phase power divider with ideal transmission, reflection, and isolation at its central frequency can be written as

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} = \begin{bmatrix} 0 & kA & -A \\ kA & 0 & 0 \\ -A & 0 & 0 \end{bmatrix} \tag{1}$$

where kA and $-A$ represent transmission coefficients of S_{12} and S_{13} of a power divider using a single resistor shown in Fig. 1, k^2 is the power ratio between port 2 and 3. If port 1 is terminated by the matched load, the S-parameter matrix of port 2 and 3 is a zero matrix

$$[S]_{23} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}. \tag{2}$$

The relationship between Y matrices of port 2 and 3 can be derived from the matrix transforming method in [18]

$$[Y]_{23} = \begin{bmatrix} Y_{T2} & 0 \\ 0 & Y_{T3} \end{bmatrix}. \tag{3}$$

where $Y_{T2,3}$ is the terminal real admittance of port 2 and 3, Z_{T2} and Z_{T3} are the terminal real impedance of port 2 and 3, and $Y_{T2,3} = 1/Z_{T2,3}$. The terminal real impedance is set to $Z_{T1} = m_1 Z_0$, $Z_{T2} = m_2 Z_0$, and $Z_{T3} = m_3 Z_0$, in which Z_{in2} and Z_{in3} are the input impedance of the power dividing network shown in Fig. 1. Accordingly, the following equations can be derived:

$$Z_{\text{in3}} = k^2 Z_{\text{in2}} \tag{4a}$$

$$\frac{1}{Z_{\text{in2}}} + \frac{1}{Z_{\text{in3}}} = \frac{1}{Z_{T1}}. \tag{4b}$$

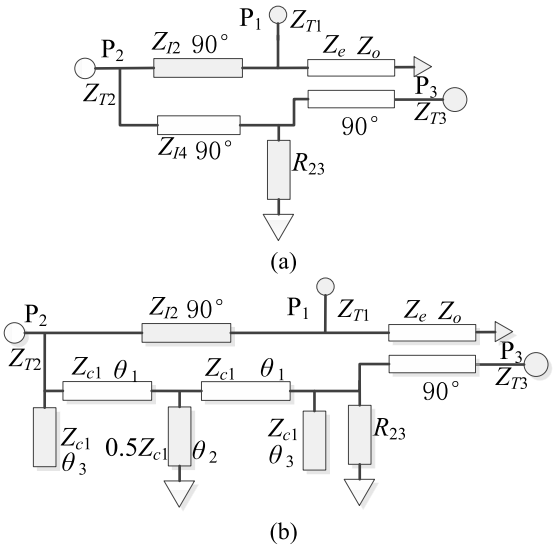


Fig. 2. Proposed out-of-phase power divider prototypes. (a) With power ratio $k^2 < 3^2$. (b) With power ratio $k^2 > 3^2$.

The Y matrices of power dividing and isolation network between port 2 and 3 are required to satisfy the following equation:

$$\begin{bmatrix} Y_{T2} & 0 \\ 0 & Y_{T3} \end{bmatrix} = \begin{bmatrix} Y_{11i} & Y_{12i} \\ Y_{21i} & Y_{22i} \end{bmatrix} + \begin{bmatrix} Y_{11d} & Y_{12d} \\ Y_{21d} & Y_{22d} \end{bmatrix}. \tag{5}$$

The subscript d and i indicate the corresponding Y matrix of power dividing and isolation network, respectively. The relation among terminal real impedance, power ratio and image impedance of the transmission line, coupled transmission line, or other equivalent networks can be determined by the following equations:

$$Z_{I2} = \sqrt{Z_{T2} Z_{\text{in2}}} = Z_0 \sqrt{m_1 m_2 \left(1 + k^2\right)} / k \tag{6a}$$

$$Z_{I3} = \sqrt{Z_{T3} Z_{\text{in3}}} = Z_0 \sqrt{m_1 m_3 \left(1 + k^2\right)}. \tag{6b}$$

Therefore, the isolation network can be determined by the power dividing network

$$[Y]_i = \begin{bmatrix} Y_{T2} & 0 \\ 0 & Y_{T3} \end{bmatrix} + \begin{bmatrix} \dfrac{Z_{T1}}{Z_{I2}^2} & \dfrac{Z_{T1}}{Z_{I2} Z_{I3}} \\ \dfrac{Z_{T1}}{Z_{I2} Z_{I3}} & \dfrac{Z_{T1}}{Z_{I3}^2} \end{bmatrix}. \tag{7}$$

B. New Out-of-Phase Power Divider

To design an out-of-phase power divider, we propose two prototypes shown in Fig. 2. As we discussed before, the even/odd mode method is not a rigorous method for asymmetric structures. There is no distinct boundary between power dividing and isolation network in Fig. 2. We cannot determine the isolation network directly from the power dividing network as (7). As a result, a new analysis method should be applied to deal with the problem.

To deal with the problem, some physical phenomena should be considered. For an ideal power divider, when power is divided from port 1 to port 2 and port 3, no power should

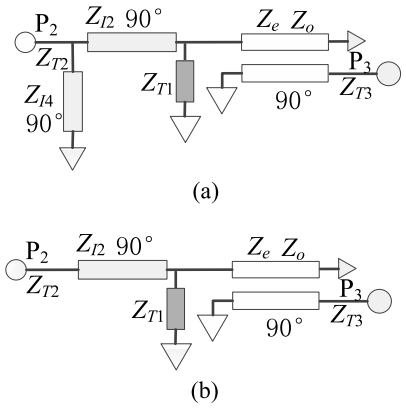


Fig. 3. (a) Equivalent power dividing network of the proposed out-of-phase power divider prototype. (b) Corresponding simplified equivalent circuit at the central frequency.

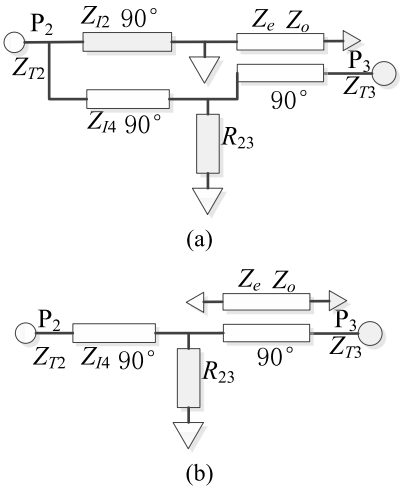


Fig. 4. (a) Equivalent power isolation network of the proposed out-of-phase power divider prototype. (b) Corresponding simplified equivalent circuit at the central frequency.

be absorbed by resistors. Namely, voltages on both sides of a resistor should be equal. Considering the proposed out-of-phase power divider prototype shown in Fig. 2, both sides of the resistor should be short-circuited to the ground. A new equivalent power dividing network is shown in Fig. 3(a). The simplified equivalent power dividing network is shown in Fig. 3(b).

The *ABCD* matrix of the power dividing network shown in Fig. 3(b) at the central frequency can be written as

$$[A]_d = [A]_{d12}[A]_{dt}[A]_{d13} = \begin{bmatrix} \dfrac{Z_{I2}}{Z_{I3}} & \dfrac{Z_{I2}Z_{I3}}{Z_{T1}} \\ 0 & \dfrac{Z_{I3}}{Z_{I2}} \end{bmatrix}. \tag{8}$$

The subscript d represents the *ABCD* matrix of the power dividing network. Z_{I3} is the image impedance at the central frequency of coupled lines in Fig. 3(b). The related Y matrix of the power dividing network can be derived as

$$[Y]_d = \begin{bmatrix} -\dfrac{Z_{T1}}{Z_{I2}^2} & -\dfrac{Z_{T1}}{Z_{I2}Z_{I3}} \\ -\dfrac{Z_{T1}}{Z_{I2}Z_{I3}} & -\dfrac{Z_{T1}}{Z_{I3}^2} \end{bmatrix} \tag{9}$$

$$Z_{I3} = \frac{2Z_eZ_o}{Z_e - Z_o}. \tag{10}$$

Next, considering a two-port network between port 2 and 3 when port 1 is terminated by the matched load, no power should be absorbed by the matched load of port 1. Consequently, voltages on both sides of the load should be equal. Comparing with the prototype shown in Fig. 2, both sides of the load should be short-circuited to the ground. A new equivalent power isolation network is shown in Fig. 4(a). The simplified equivalent power isolation network is shown in Fig. 4(b).

The *ABCD* matrix of the power isolation network shown in Fig. 4(b) at the central frequency can be written as

$$[A]_i = [A]_{i12}[A]_{it}[A]_{i13} = \begin{bmatrix} -\dfrac{Z_{I4}}{Z_{I5}} & -\dfrac{Z_{I4}Z_{I5}}{R_{23}} \\ 0 & -\dfrac{Z_{I5}}{Z_{c4}} \end{bmatrix} \tag{11}$$

where the subscript i indicates the *ABCD* matrix of power isolation network, and Z_{I5} is the image impedance at the central frequency of coupled lines shown in Fig. 4(b), which is determined by the following equation:

$$Z_{I5} = \frac{2Z_eZ_o}{Z_e + Z_o}. \tag{12}$$

The related Y matrix of the power isolation network can be derived as

$$[Y]_i = \begin{bmatrix} \dfrac{R_{23}}{Z_{I4}^2} & \dfrac{R_{23}}{Z_{I4}Z_{I5}} \\ \dfrac{R_{23}}{Z_{I4}Z_{I5}} & \dfrac{R_{23}}{Z_{I5}^2} \end{bmatrix}. \tag{13}$$

Substituting (9) and (13) into (7), the following equations can be derived:

$$\frac{R_{23}}{Z_{c4}Z_{I5}} = \frac{Z_{T1}}{Z_{I2}Z_{I3}} \tag{14a}$$

$$Y_{T2} = \frac{R_{23}}{Z_{I4}^2} - \frac{Z_{T1}}{Z_{I2}^2} \tag{14b}$$

$$Y_{T3} = \frac{R_{23}}{Z_{I5}^2} - \frac{Z_{T1}}{Z_{I3}^2}. \tag{14c}$$

All terminal real impedances are set to $Z_{T1} = m_1Z_0$, $Z_{T2} = m_2Z_0$, $Z_{T3} = m_3Z_0$, other main parameters are set to $Z_e = m_eZ_0$, $R_{23} = m_4Z_0$. Substituting (6), (10), and (12) into (14), the following equations can be used to determine those related parameters in Fig. 2:

$$Z_o = \frac{m_eZ_0\sqrt{\left(m_1m_3\left(1+k^2\right)\right)}}{2m_e + \sqrt{\left(m_1m_3\left(1+k^2\right)\right)}} \tag{15a}$$

$$m_4 = \frac{m_1m_e^2k^2Z_0}{\left[m_e + \sqrt{\left(m_1m_3\left(1+k^2\right)\right)}\right]^2} \tag{15b}$$

$$Z_{c4} = \frac{m_ekZ_0\sqrt{\left(m_1m_2\left(1+k^2\right)\right)}}{\left[m_e + \sqrt{\left(m_1m_3\left(1+k^2\right)\right)}\right]}. \tag{15c}$$

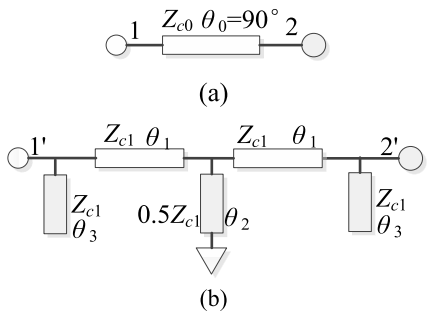


Fig. 5. (a) 90° electrical length transmission line. (b) Its equivalent circuit.

C. Equivalent High Image Impedance Microstrip Line

According to the above discussion, it can be found that the power ratio of a power divider is restricted by the available characteristic impedance of microstrip lines, which are further limited by the fabrication process of planar printed circuit board (PCB). In order to design a high impedance transmission line, we suggest employing another equivalent circuit. A 90° electrical length transmission line and its equivalent circuit are shown in Fig. 5. The even-/odd-mode method is applied to analyze the relations in each transmission line. If two two-port networks shown in Fig. 5 are equivalent to each other at the central frequency, the even-/odd-mode admittance should satisfy

$$Y'_{\text{in}o} = Y_{\text{in}o} \tag{16a}$$

$$Y'_{\text{in}e} = Y_{\text{in}e} \tag{16b}$$

where the prime $'$ refers to the equivalent circuit in Fig. 5(b), subscript in o and in e refer to odd-mode and even-mode input admittance. According to Fig. 5, the following equations can be written as:

$$Y_{\text{in}o0} = -jY_{c0}\cot\theta_0 \tag{17a}$$

$$Y_{\text{in}e0} = jY_{c0}\tan\theta_0 \tag{17b}$$

$$Y'_{\text{in}o1} = jY_{c1}\tan\theta_3 - jY_{c1}\cot\theta_1 \tag{17c}$$

$$Y'_{\text{in}e1} = jY_{c1}\tan\theta_3 - jY_{c1}\cot(\theta_1+\theta_2). \tag{17d}$$

To simplify notations, the following parameters are set to $\theta_1 = 45°$, $m_c = Y_{c1}/Y_{c0}$. Substituting (17) into (16), the following relations can be derived:

$$\tan\theta_3 = 1 - \frac{1}{m_c} \tag{18a}$$

$$\tan\theta_2 = \frac{1}{2(m_c-1)}. \tag{18b}$$

According to the theoretical analysis, the design procedure for the proposed out-of-phases power divider with arbitrary terminal real impedance with coefficients m_1, m_2, m_3, and arbitrary power ratio k^2 can be summarized as follows.

1) First, calculate the characteristic image impedance of Z_{I2}, and image impedance Z_{I3} of coupled microstrip lines from terminal real impedance and power ratio k^2 by (6). If the calculated image impedance is less than 120 Ω, a section of microstrip line shown in Fig. 5(a) can be selected. If the image impedance is larger than 120 Ω, an equivalent high impedance circuit shown in Fig. 5(b) can be used, whose parameters can be calculated by (18).
2) Calculate the odd mode characteristic impedance of coupled microstrip lines from the even mode characteristic impedance with coefficient m_e, terminal real impedance, and power ratio k^2 by (15a).
3) Calculate the values of resistors from the even mode characteristic impedance, terminal real impedance R_{23}, and the power ratio by (15b).
4) Calculate the characteristic impedance of Z_{I4} from even mode characteristic impedance, terminal real impedance, and power ratio by (15c).
5) According to those available values of Z_e and resistors in the resistor bag, tune m_e to meet the design goal.

TABLE I
MAIN PARAMETERS OF PROPOSED POWER DIVIDER WITH $k^2 < 3^2$

k	Z_e	Z_o	Z_{c2}	Z_{c4}	R_{23}
1.00	50.00	20.71	70.71	29.29	8.58
2.00	50.00	26.39	55.90	69.10	19.13
3.00	50.00	30.63	52.70	113.96	25.97

III. TWO OUT-OF-PHASE POWER DIVIDERS

The proposed out-of-phase power dividers are calculated by the ideal transmission line and lumped components with different power ratios k^2 at the central frequency of 2.0 GHz. Different terminal real impedances of the proposed power dividers are not further discussed.

A. Out-of-Phase Power Divider With Ratio $k^2 < 3^2$

To design an out-of-phase power divider with power ratio $k^2 < 3^2$, the proposed out-of-phase power divider prototype in Fig. 2(a) is used.

Parameters of the proposed power divider 1 (confined as E1 in this article) are set to $m_1 = m_2 = m_3 = m_e = 1$, other main parameters are listed in Table I.

The calculated scattering parameters of E1 are shown in Fig. 6(a) and (b). The operation bandwidth is defined that all S_{11}, S_{22}, S_{23}, S_{33} are better than −15 dB, S_{12} is better than $10*\log_{10}(k^2/(1+k^2)) \pm 1$ dB, and S_{13} is better than $10*\log_{10}(1/(1+k^2)) \pm 1$ dB. Accordingly, we find that the −15-dB bandwidth for reflection and isolation is 1.67–2.33 GHz with a fractional bandwidth (FBW) about 33% for $k = 1$, 1.60–2.40 GHz with FBW about 40% for $k = 2$, and 1.59–2.61 GHz with FBW about 41% for $k = 3$, respectively.

The amplitude and phase unbalance results are plotted in Fig. 6(c). In 1.67–2.33 GHz for $k = 1$, amplitude unbalance is better than 0.26 dB, phase unbalance is better than 0.32°. In 1.60–2.40 GHz for $k = 2$, amplitude unbalance is better than −0.14 dB + 6.02 dB, phase unbalance is better than 5.39°. In 1.59–2.61 GHz for $k = 3$, amplitude unbalance is better than −0.14 dB + 9.54 dB, phase unbalance is better than 6.85°. According to the figure, we find the circuit model with $k = 1$ showing better phase unbalance performance.

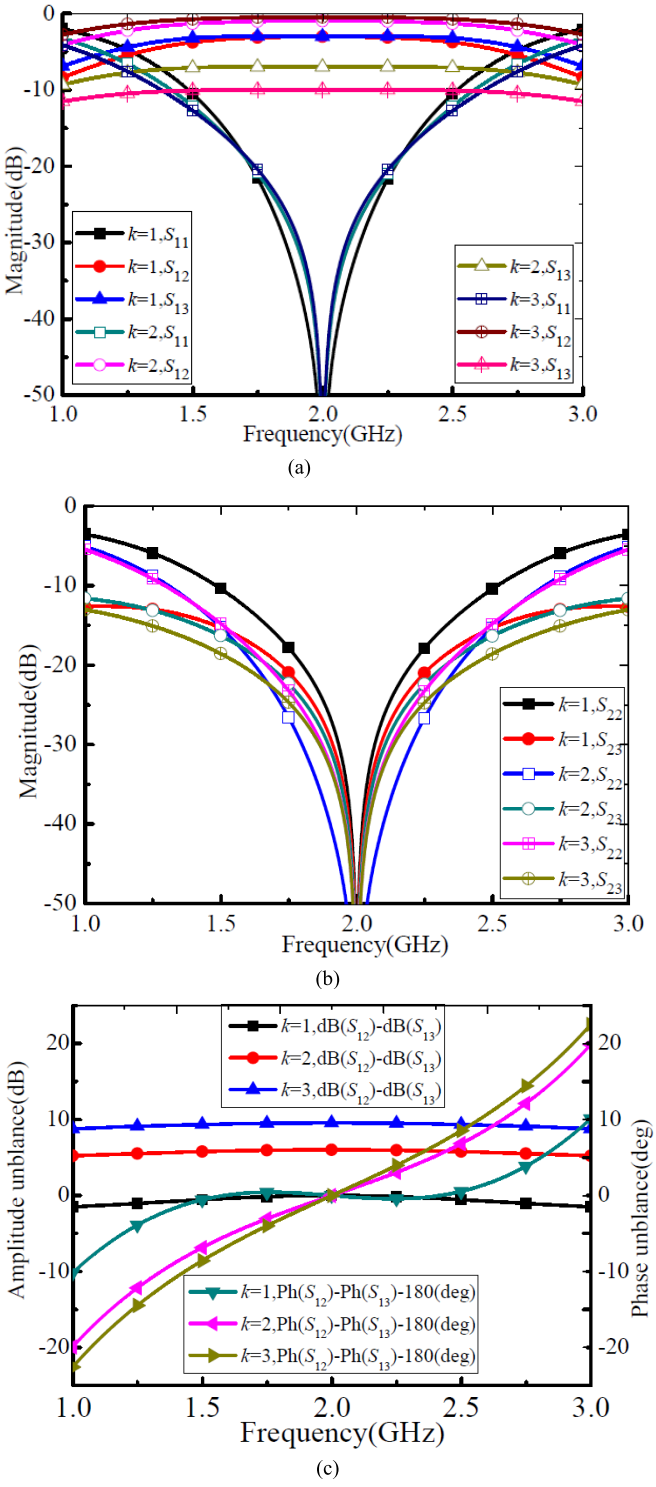


Fig. 6. (a) Calculated scattering parameters S_{11}, S_{12}, and S_{13} of the first group of the circuit model ($m_1 = m_2 = m_3 = 1$) depicted in Fig. 2. (b) Calculated S_{22}, S_{23} of the first group of the circuit model shown in Fig. 2. (c) Amplitude and phase unbalance of the first group of the circuit model shown in Fig. 2. "Ph()" refers to phases of S_{12}, S_{13} with the unit of degree, and "dB()" refers to amplitudes of S_{12}, S_{13}. The same legend is applied in the following figures.

B. Out-of-Phase Power Divider with ratio $k^2 > 3^2$

To design an out-of-phase power divider with ratio $k^2 > 3^2$, the proposed out-of-phase power divider prototype in Fig. 2(b) is used.

TABLE II
MAIN PARAMETERS OF PROPOSED POWER DIVIDER $k^2 > 3^2$

k	Z_o	Z_{c2}	θ_2	θ_3	R_{23}
3.16	32.03	52.44	62.95	11.50	28.65
10.0	43.21	50.25	7.64	38.26	44.26
31.60	48.96	50.02	1.91	43.15	51.00

Parameters of proposed power divider 2 (confined as E2) are set to $m_1 = m_2 = m_3 = m_e = 1$, $Z_{c1} = 100\ \Omega$, other main parameters are listed in Table II.

The calculated scattering parameters of E2 with ideal components are shown in Fig. 7(a) and (b). If the bandwidth is defined the same with the previous case, we find that the -15 dB bandwidth for reflection and isolation is 1.58–2.42 GHz with FBW about 42% for $k = 3.16$, 1.56–2.44 GHz with FBW about 44% for $k = 10$, and 1.56–2.64 GHz with FBW about 44% for $k = 31.6$.

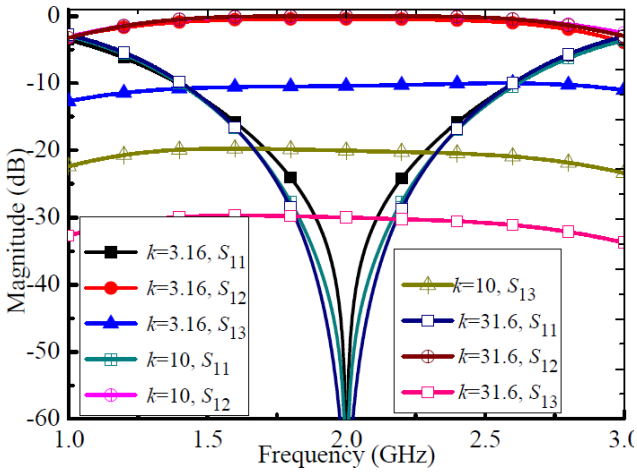
The amplitude and phase unbalances are plotted in Fig. 7(c). According to the figure, we find that the circuit model with $k = 1$ shows better phase performance. In 1.58–2.42 GHz for $k = 3.16$ (the power ratio equals to 10 dB), the amplitude unbalance is better than ± 0.1 dB + 10 dB, the phase unbalance is better than $\pm 1.68°$. In 1.56–2.44 GHz for $k = 10$ (power ratio equals to 20 dB), amplitude unbalance is better than ± 0.45 dB + 20 dB, and phase unbalance is better than $\pm 7.35°$. In 1.56–2.64 GHz for $k = 31.6$ (power ratio equals to 30 dB), the amplitude unbalance is better than ± 0.45 + 30 dB, and the phase unbalance is better than $\pm 9.79°$. According to the figure, we find the circuit model with $k = 3.16$ showing better phase unbalance performance. From Fig. 7(c), phase imbalance deteriorates with the increasing of k. FBW increases as the characteristic impedance Z_{c1} increases from Fig. 8.

IV. RESULTS AND DISCUSSION

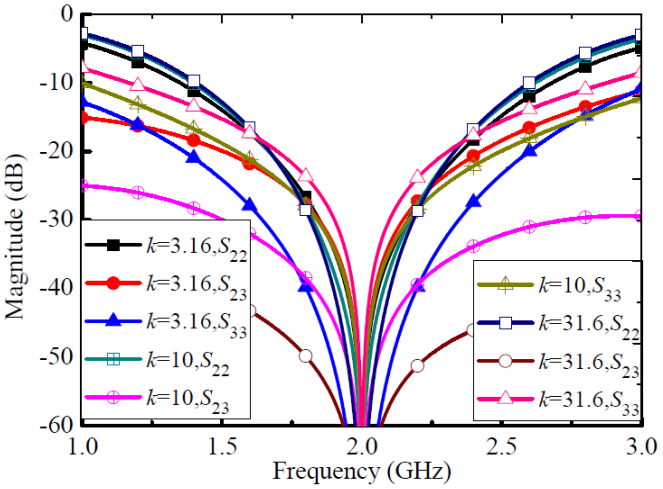
To verify the proposed method, power divider E1 with $f_0 = 2$ GHz, $k = 3$, is simulated and fabricated on the microstrip PCB Rogers RO4350B with $\varepsilon_r = 3.66$ and tan $\delta = 0.0031$. The thicknesses of the dielectric layer and the metal layer are given by $h = 0.508$ mm and $t = 0.0035$ mm, respectively. The initial values of impedances and resistors shown in Fig. 3(a) are set to $Z_e = 50.7\ \Omega$, $Z_o = 31.4\ \Omega$, $Z_{c2} = 52.7\ \Omega$, $Z_{c4} = 116.3\ \Omega$, and $R_{23} = 27.1\ \Omega$.

By simple tuning and optimizing, the dimensions are shown in Fig. 9 with $W_0 = 1.10$ mm; $W_1 = 0.17$ mm, $L_1 = 22.13$ mm; $W_{c1} = 1.35$ mm, $L_{c1} = 22.42$ mm, $g_{c1} = 0.16$ mm; $W_{c2} = 1.19$ mm, $L_{c2} = 20.95$ mm, $g_{c2} = 0.40$ mm, and $r = 0.25$ mm. The diameter of the metal cylindrical via is 0.5 mm. L_3 refers to the distance between the center of the metal cylindrical via and the intersection of the T-junction. The resistor with specification of 0603 is 27 Ω. The total size is $0.50 \times 0.05\ \lambda_g^2$.

As demonstrated in Fig. 10, the frequency range is 1.526–2.442 GHz whereas all S_{11}, S_{22}, S_{23}, S_{33} are better than -15 dB, S_{12} is better than -0.46 dB $\pm$ 1 dB, and S_{13} is better than -10 dB $\pm$ 1 dB for simulated results with a FBW



(a)



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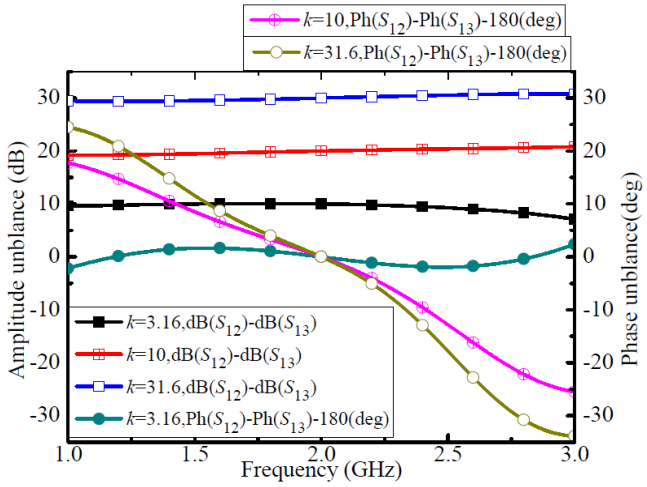

(c)

Fig. 7. (a) Calculated scattering parameters S_{11}, S_{12}, S_{13} of the proposed power divider 1 with ideal components shown in Table I and Fig. 2(b). (b) Calculated S_{22}, S_{23} of the first group of the circuit model shown in Fig. 2(b). (c) Amplitude and phase unbalances of the proposed power divider 1 shown in Fig. 2(b).

of 45.8%. The frequency range is 1.528–2.376 GHz whereas S_{11}, S_{22}, S_{23} are better than −15 dB, and S_{33} is better than −14.42 dB for measured results with a FBW of 42.2%.

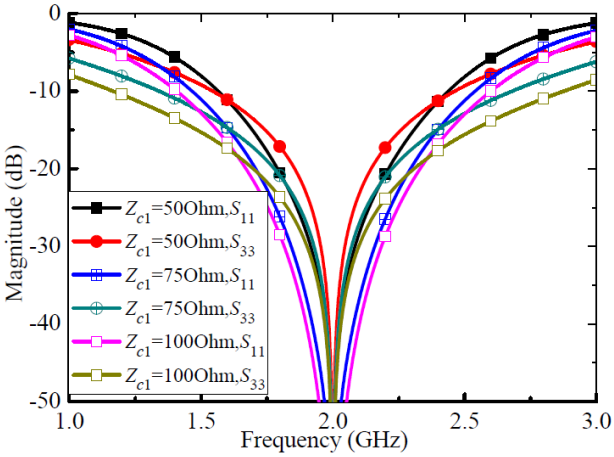

Fig. 8. Calculated scattering parameters S_{11} and S_{32}, for $k_2 = 1000$ with different Z_{c1}.

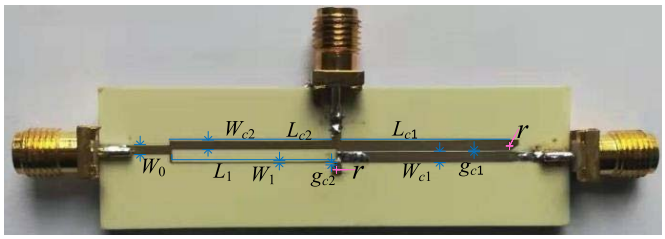

Fig. 9. Proposed out-of-phase power divider on microstrip lines with power ratio $k^2 = 9$.

In 1.526–2.442 GHz, simulated amplitude unbalance is below 9.46 dB ± 0.3 dB, and simulated phase unbalance is below 9.4° in Fig. 11. In 1.528–2.376 GHz, measured amplitude unbalance is below 9.46 ± 0.3, and measured phase unbalance is below 10.7°.

Power divider E2 with $f_0 = 2$ GHz, $k = 31.6$ (power ratio equals to 30 dB), is simulated and fabricated on the microstrip PCB Rogers RO4350B with $\varepsilon_r = 3.66$ and tan $\delta = 0.0031$. The thicknesses of the dielectric layer and the metal layer are given by $h = 0.762$ mm and $t = 0.0035$ mm, respectively. The initial values of impedances and resistor shown in Fig. 3(b) are set to $m_e = 1.04$, $Z_e = 52.19\ \Omega$, $Z_o = 48.96\ \Omega$, $Z_{c2} = 50.03\ \Omega$, $Z_{c4} = 1597.68\ \Omega$, and $R_{23} = 51.00\ \Omega$.

After tuning and optimizing, the dimensions are shown in Fig. 12 with $W_0 = 1.56$ mm; $W_1 = 0.36$ mm, $L_1 = 11.63$ mm, $L_2 = 1.14$ mm, $L_3 = 10.61$ mm; $W_{c1} = 1.80$ mm, $L_{c1} = 22.22$ mm, $g_{c1} = 1.92$ mm; $W_{c2} = 1.68$ mm, $L_{c2} = 22.15$ mm, and $r = 0.25$ mm. The surface mounted technology (SMT) resistor with specification of 0603 is 51 Ω. The total size is $0.50 \times 0.08\ \lambda_g^2$.

As demonstrated in Fig. 13, the frequency range is 1.762–2.357 GHz to preserve that all S_{11}, S_{22}, S_{23}, S_{33} are better than −15 dB, S_{12} is better than −0.46 ± 1 dB, and S_{13} is better than −30.46 ± 1 dB for simulated results with an FBW of 29.7%. The frequency range is 1.811–2.214 GHz that S_{11}, S_{22}, S_{23}, and S_{33} are better than 15 dB for measured results with an FBW of 20.2%.

As demonstrated in Fig. 14, in 1.762–2.357 GHz, the simulated amplitude unbalance is below 30 ± 3.16 dB, and the simulated phase unbalance is below 12.8°. In

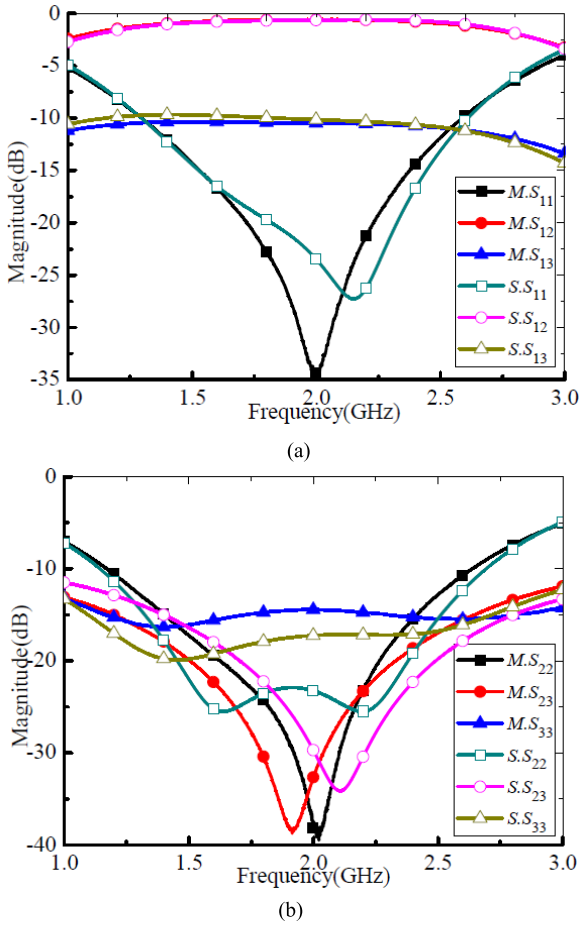

Fig. 10. Simulated and measured scattering parameters of the proposed power divider with power ratio $k^2 = 3^2$. (a) S_{11}, S_{12}, S_{13}. (b) S_{22}, S_{23}, S_{33}.

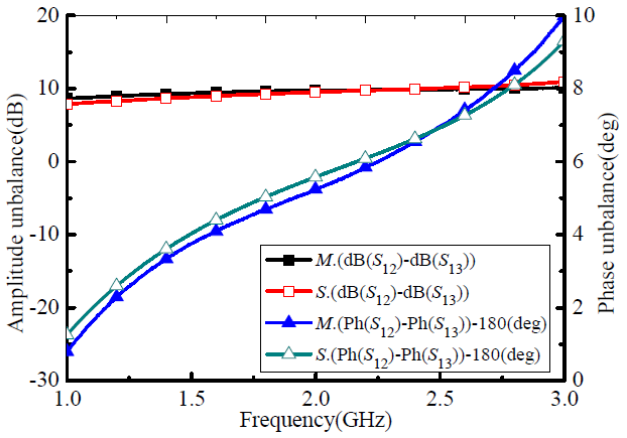

Fig. 11. Simulated and measured amplitude and phase unbalances of the proposed power divider with power ratio $k^2 = 3^2$.

1.811–2.214 GHz, the measured amplitude unbalance in Fig. 13 is below 30 ± 0.82 dB, and the measured phase unbalance is below 7.0°. In Figs. 10 and 13, the frequency shift in simulated and measured scattering parameters, for example, S_{23}, is mainly due to the compact size, and interdependence between power dividing and isolation networks. Other reasons include fabrication errors, inhomogeneous material, and the error of resistor values. Fabrication errors in the compact device will magnify the frequency shift between simulated

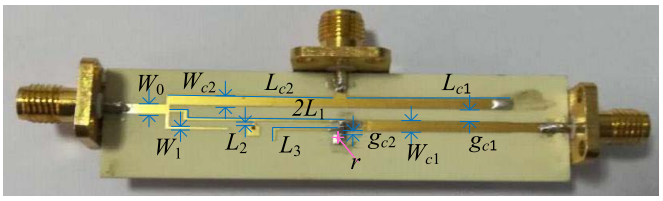

Fig. 12. Proposed out-of-phase power divider on microstrip lines with power ratio $k^2 = 1000$.

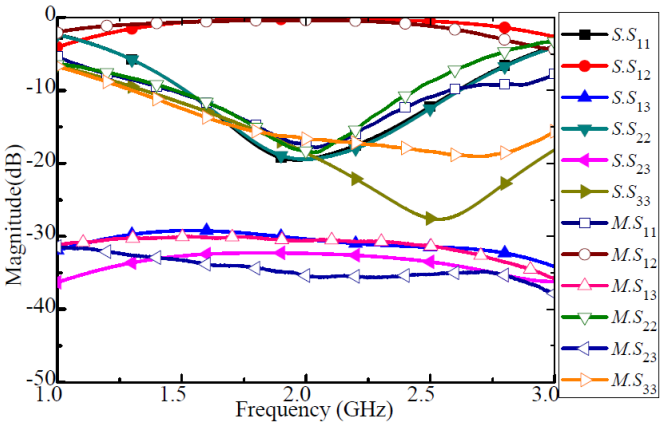

Fig. 13. Simulated and measured scattering parameters of the proposed power divider power ratio $k^2 = 31.6^2$.

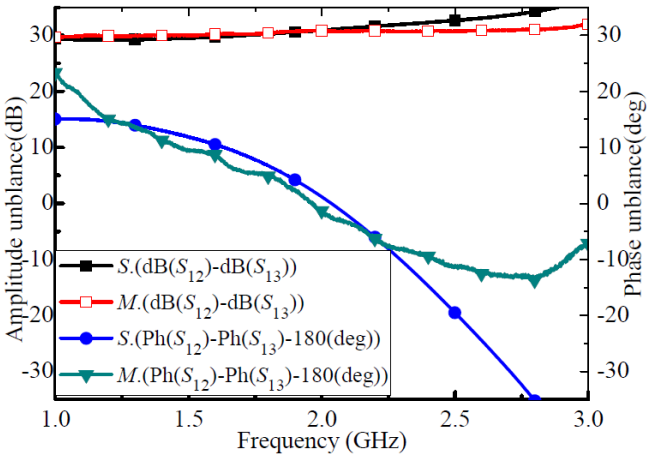

Fig. 14. Simulated and measured amplitude and phase unbalances of the proposed power divider with power ratio $k^2 = 1000$.

and measured results. This is because the discontinuity, the fabrication, the inhomogeneous material, and resistor errors have not been completely included in simulation and calculation.

To demonstrate the advantages of this design, a comparison is given in Table III. From Table III, one can find that this design has realized arbitrary power ratio with compact size. The proposed design is the first work to provide 30-dB power ratio with compact size. Besides, the proposed design method can be used to deal with arbitrary terminal real impedance with same topology. It should be noted that FBW in the table is defined as FBW that satisfies additional insertion loss below −1 dB, reflection and isolation loss better than −15 dB, except for E1 whose FBW is defined by reflection and isolation loss better than −14.42 dB.

TABLE III
COMPARISON BETWEEN THE PROPOSED DESIGNS WITH OTHER WORKS

Refs	f_0	-IL(dB).	FBW .(%)	dB (k^2)	Fab.	Size ($\lambda_g \times \lambda_g$)
[6]	2	0.85/10.9	16	10	MS.	0.6*0.3
[19]	2.5	0.19/20.65	8.1	20	MS.	0.6*0.2
[20]	2	0.75/10.29	16	10	MS.	0.3*0.3
[21]	2	1.45/11.45	<5	10	MS.	0.2*0.28
[22]	1	-	-	20	MS.	0.2*0.2
[23]	1	-	-	20	MS.	0.2*0.3
[24]	1.5/ 2.4	-	27	1	DSPSL	0.5*0.2
[25]	3	4.03-4.21	64.8	1	MS./Sl.	0.5*0.3
[26]	6	4-5.2	110	1	MS./Sl.	0.6*0.6
[27]	3	4.8	60	1	MS./Sl.	0.5*0.6
E1.	2	0.86/10.72	42.2	9.54	MS.	0.46*0.03
E2.	2	0.34/31.06	20.2	30	MS.	0.46*0.05

MS. refers to Microstrip, Sl. refers to Slot, E1 and E2 are two examples in this paper.

V. CONCLUSION

A new design of an out-of-phase power divider is proposed to provide more compact size. We derive the relations between the equivalent power dividing and isolation networks by Y matrix to determine parameters of the power divider. Arbitrary power ratio has been discussed for the proposed dividers. Based on the design procedure, we have designed two power dividers with compact size. The proposed two power dividers are fabricated on Rogers RO4350 to realize power ratio of $k^2 = 3^2$ and $k^2 = 1000$. The amplitude and phase performance is demonstrated by the simulated and measured S-parameters, indicating that the proposed prototype will be very useful in the compact RF circuits.

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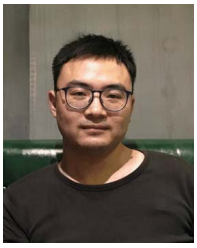

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